IN THE CLAIMS

Please amend claims 1, 8 and 16 as indicated below.

Please cancel claims 22-32 without prejudice or disclaimer.

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claim 1 (currently amended) A switch comprising:

[[A]] a plurality of ports for exchanging data, and a shared-memory for enabling the exchange of data between first and second ones of said ports, said shared-memory comprising:

[[An]] an array of memory cells arranged as a plurality of rows and a single column having a width equal to a predetermined word-width;

[[Circuitry]] circuitry for writing selected data presented at said first one of said ports to a selected row in said array as a word of the predetermined word-width during a first time period and for reading said selected data as a word of the predetermined word-width from said selected row during a second time period for output at said second one of said ports.

Claim 2 (original) The switch of Claim 1 and further comprising a buffer associated with each port for converting words of data from an initial bit-width to said predetermined bit width.

Claim 3 (original) The switch of Claim 1 wherein said predetermined bit-width is equal to a bit-width of certain bit width and associated overhead.

Claim 4 (original) The switch of Claim 2 wherein said initial bit-width is 48 bits and said predetermined bit-width is 384 bits.

Claim 5 (original) The switch of Claim 1 wherein said circuitry for reading and writing comprises an available address table for storing write addresses available for selection and use in writing to selected rows said array.

Claim 6 (original) The switch of Claim 5 wherein said circuitry for reading and writing further comprises a used address table for storing addresses already used for writing data to selected rows in said array.

Claim 7 (original) The switch of Claim 1 wherein said array comprises an array of random access memory cells of the read/write classification.

Claim 8 (currently amended) A shared-memory switch comprising:

[[A]] a plurality of ports for exchanging data between external devices associated with each of said ports;

[[A]] a buffer associated with each of said ports for assembling a stream of data words being input into said switch into a single word of a predetermined width and for converting single data words of said predetermined width being output from said switch into a stream of data words;

[[A]] a shared-memory for effectuating a transfer of data from a first one of said ports to a second one of said ports through corresponding ones of said buffers, said shared-memory comprising a plurality of banks each having an array of memory cells arranged as a plurality of rows and a single column of said predetermined width and circuitry for selecting a said row in response to a received address;

[[A]] a plurality of available address tables each for maintaining a queue of addresses available for writing said single words of data to a corresponding one of said banks; and

[[A]] a plurality of used address tables each for maintaining a queue of addresses for reading from a corresponding one of said banks.

Claim 9 (original) The switch of Claim 8 wherein said streams of data words comprise eight forty-eight bit words of ATM data and said single words have a said predetermined width of 384 bits.

Claim 10 (original) The switch of Claim 8 wherein each of said plurality of available address tables comprises a first-in-first-out memory.

Claim 11 (original) The switch of Claim 8 wherein each of said plurality of used address tables comprises a random access memory, that performs read and write operations.

Claim 12 (original) The switch of Claim 8 wherein each of said banks is randomly accessible.

Claim 13 (original) The switch of Claim 8 wherein each of said banks stores data corresponding to a selected said port from which data is to be read.

Claim 14 (original) The switch of Claim 8 wherein each of said banks stores data corresponding to a plurality of ports from which data is to be read in a selected order.

Claim 15 (original) The switch of Claim 8 wherein said shared-memory comprises i number of banks and said switch comprises j number of ports, where $i < j$.

Claim 16 (currently amended) A digital information system comprising:

[[First]] first and second resources operable to exchange data in a selected digital format; and

[[A]] a digital switch comprising:

[[First]] first and second ports for selectively coupling said first and second resources; and

[[A]] a shared memory for enabling the exchange of data between said first and second ports as words of a predetermined word-width, said shared-memory comprising:

[[An]] an array of memory cells arranged as a plurality of rows and a single column having a width equal to said predetermined word-width; and

[[Circuitry]] circuitry for writing a selected data word presented at said first one of said ports to a selected row in said array during a first time period and for reading said selected data word from said selected row during a second time period to said second one of said ports.

Claim 17 (original) The system of Claim 16 wherein data are exchanged through said ports as streams of data words of an initial word-width and said switch further comprises buffers for converting data words between said initial word-width and said predetermined word-width.

Claim 18 (original) The system of Claim 16 wherein said selected digital format comprises as Asynchronous Transfer Mode digital data format.

Claim 19 (original) The system of Claim 18 wherein said predetermined word-width equals a bit-width of a user data portion of an asynchronous transfer mode information packet.

Claim 20 (original) The system of Claim 16 wherein said first and second resources are selected from the group comprising digital telephones, digital facsimile machines, digital data networks, home networks, digital private branch exchanges, workstations and video teleconferencing equipment.

Claim 21 (original) The system of Claim 16 where the data interface is selected from the group consisting of DDR (double data rate), QDR (quad data rate), Rambus™, and programmable bit burst length interfaces.

Claims 22-32 (cancelled)